A State Variable Method of Circuit Analysis Based on a Nodal Approach

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A method which is well suited for implementation on a digital computer is presented for the solutions of active circuits. Unlike many state variable approaches the state vector is defined as the set of voltages which exist between certain nodes and the reference node. An advantage of this approach is that degeneration in the order of complexity of the network caused by capacitance loops is handled automatically. Any type of controlled source can be specified. From the basic algorithm the circuit is specified in matrix form by inspection using standard nodal methods, and the solution is obtained by a systematic reduction of this one matrix equation. An upper bound on the order of complexity of the network is evident from the network topology or the partitioned form of the original matrix. Inductors are included in this approach by considering the equivalent gyrator-capacitor combination.

I. INTRODUCTION

State variable techniques presently being used to analyze networks require a detailed knowledge of graph theory.[1–7] Another method of state variable analysis that is based partly on a nodal approach and does not require a detailed knowledge of graph theory is very restrictive.[8] The method presented here performs a nodal analysis on a transformation of the network in which all magnetic storage elements have been replaced by gyrator-capacitor equivalents, and nothing more than a basic knowledge of graph theory nomenclature is required. The RCLMST* network can be transformed to an equivalent

* Resistor, capacitor, inductor, mutual inductor, source and ideal transformer.

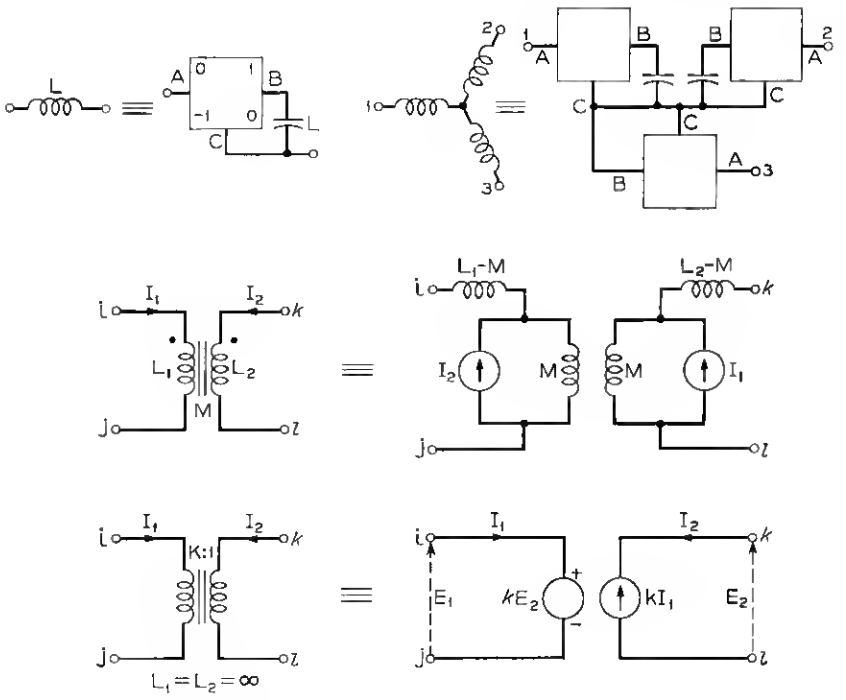

Fig. 1 — Inductor and transformer equivalents.

resistance capacitance source network using the gyrator-capacitor equivalents shown in Fig. 1. Each gyrator shown in Fig. 1 has the indefinite admittance parameters

$$\begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 \\ -1 & 0 & 1 \\ 0 & -1 & 0 \end{bmatrix} \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix};$$

choosing this type of gyrator enables the capacitor value in farads of the equivalent pair to be equal to the inductor value in henries.

Let the number of nodes of a transformed network be n. Using Kirchoff's current law, it can be shown that for an n-node RCS network

$$C\dot{\mathbf{V}} = \mathbf{I} - G\mathbf{V} \tag{1}$$

where $\mathbf{I}$ is an $(n-1)$th ordered column vector representing the currents

injected into the nodes, V is an $(n-1)$th ordered column vector representing the voltages between the nodes of the network and the reference node. If the transformed network contains l capacitors then the matrix C is an $(n-1)$th ordered symmetric matrix which contains imbedded within it l second order indefinite matrices, each having the dimensions of farads. Similarly G represents the resistors and has the dimensions of mhos, but G may be asymmetric. Node n is the common or ground node of the network; for convenience this node is always assumed to have capacitors connected to it.

The objective is to find an upper bound on the rank of the capacitance matrix C by partitioning C as described in Section II, and reducing the matrix equation (1) containing the partitioned matrix C to the rank of C; this reduction is symbolic and does not take into account degenerate cases which can occur. It is shown in Appendix B that for all conditions, for any type of circuit, an upper bound on the order of complexity of the network (rank of C) can be found from the network topology.

II. PARTITIONING OF THE CAPACITANCE MATRIX

There are basically four types of voltage source (VS), the independent VS (IVS), the voltage dependent VS (VDVS), the current dependent VS where the current is through a resistor (CDVSR), and the current dependent VS where the current is through a capacitor (CDVSC). It will be shown that the only current source (CS) which can effect the partitioning is the current dependent CS where the current is through a capacitor (CDCSC). As a result, any type of CS will be termed simply a CS, unless it is a CDCSC.

The method of partitioning makes the reduction of the matrix equation (1) to its rank a simple process. Generally only the voltage at a node to which a capacitor is connected can be a state variable node. However it is possible to choose a node to which a CDCSC or CDVSC is connected as a state variable node instead of one of the nodes of the capacitor whose current supplies the dependence, but this possibility is avoided automatically in the partitioning method presented here.

The presence of inductors and time-invariant, independent CS's forming a cut-set in the original untransformed network causes a linear dependence problem in the transformed network. In the transformed network such a cut-set appears as a capacitor tree with gyrators only connected to the end nodes of the tree as shown in Fig. 1,

and gyrators and perhaps time-invariant independent c.s.'s connected to the central node (the GCNODE); the nodes of this capacitor tree will be called the GCSET nodes.

The capacitors in the transformed network can be divided into two classes, those connected to the reference node directly or through a vs-capacitor chain (the fixed capacitors), and those not so connected (the floating capacitors). The m floating capacitor subgraphs are defined as the m unconnected subgraphs obtained from the floating capacitor plus imbedded vs graph of the transformed network.

The partitioning of the capacitance matrix will be related to the example of Appendix A in the discussion that follows. Partition the matrix C as

$$\begin{array}{c} \\ \mathbf{n1} \\ \mathbf{n2} \\ \mathbf{n3} \\ \mathbf{n4} \\ \mathbf{n5} \end{array} \begin{array}{c} \begin{array}{ccccc} \mathbf{n1} & \mathbf{n2} & \mathbf{n3} & \mathbf{n4} & \mathbf{n5} \end{array} \\ \begin{bmatrix} C_{11} & C_{12} & C_{13} & 0 & C_{15} \\ C_{21} & C_{22} & C_{23} & 0 & C_{25} \\ C_{31} & C_{32} & C_{33} & 0 & C_{35} \\ 0 & 0 & 0 & 0 & 0 \\ C_{51} & C_{52} & C_{53} & 0 & C_{55} \end{bmatrix} \end{array}$$

where

(*i*) The nodes **n1** are all the nodes to which capacitors are connected omitting the following nodes:

(*a*) A node for each vs imbedded in a capacitor chain (these nodes are in the **n2** section), but each capacitor must be specified by at least one node.

(*b*) A node for each of the m floating capacitor subgraphs (these nodes being in the **n3** section).

(*c*) A node for each GCSET which is specified in section **n2**.

In the example in Appendix A, **n1** contains nodes $1 \rightarrow 9$.

(*ii*) The nodes **n2** represent:

(*a*) A node for each DVS imbedded in a capacitor chain.

(*b*) A node free of capacitors for each CDVSC and CDCSC free of capacitors on at least one node.

(*c*) A node for each GCSET.

In the Appendix A example **n2** contains nodes 10 and 11.

(*iii*) Section **n3** contains a node for each of the m floating capacitor subgraphs.

In the example **n3** contains nodes 12 and 13.

(*iv*) Section **n4** contains the nodes to which only resistors and CS's (but not CDCSC) are connected, including a node for each IVS, VDVS or CDCSC free of capacitors, other CDVSC's or CDCSC's on both nodes. (The other nodes of these sources are specified in section **n5**).

In the example **n4** has no entries.

(*v*) Section **n5** contains all the remaining nodes. These are:

(*a*) A node for each IVS.

(*b*) A node free of capacitors for each VDVS or CDVSR free of capacitors or CDVSC or CDCSC on at least one node.

In the example **n5** contains node 14.

The rank of the C matrix is **n1**, and **n1** = 9 for the example of Appendix A. Notice that the presence of capacitance loops in no way alters the method of partitioning.

III. REDUCTION OF THE CIRCUIT DESCRIPTION TO A MINIMAL FORM

Theorem: *An upper bound on the order of complexity of a network is the order of* **n1**.

This theorem is proved in Appendix B, where it is shown that every row in sections **n2**, **n3**, **n4**, and **n5** is linearly dependent on rows in section **n1**; the subspace spanned by sections **n2**, **n3**, **n4**, and **n5** is contained in **n1**.

The systematic reduction of equation (1) is accomplished by first eliminating section **n5** by applying the voltage restrictions caused by the VS's in section **n5**. Secondly, section **n4** is eliminated using the fact that these nodes are free of capacitors. Next, section **n3** is eliminated to correct the over specification of the floating capacitor subgraphs. Finally, the remaining dependencies of the system are caused by the DVS's imbedded in capacitive chains, the CDVSC and CDCSC free of capacitors on at least one node, and a node for each capacitive tree in which a GCSET has occurred; these dependencies are eliminated with section **n2**, yielding equation (9) of Appendix B.

Equation (9) of Appendix B can be written as

$$\dot{\mathbf{v}}\mathbf{1} = \mathbf{B} - \mathbf{A}\mathbf{v}\mathbf{1} \tag{2}$$

where

$$\mathbf{v} = \begin{bmatrix} \mathbf{v1} \\ \mathbf{v2} \\ \mathbf{v3} \\ \mathbf{v4} \\ \mathbf{v5} \end{bmatrix}$$

and **v1** is the voltage vector for nodes **n1, n2, n3,** etc.

An example of a solution based on the problem set by Pottle is given in Appendix C.

IV. CONCLUDING REMARKS

A state variable technique has been described that offers two advantages over traditional methods:

(*i*) The network can be specified completely by inspection using well known nodal techniques with little skill required, the problem then becoming one of simple matrix reduction (easily programmed for a digital computer).

(*ii*) Capacitor loops present no problem and are not even recognized as such since the partitioning and matrix reduction are unaltered if there are any capacitor loops present.

The main disadvantages are that currents must always be expressed as functions of node voltages and inductors must be replaced by gyrators and capacitors; inductor cut-sets must be recognized and the circuit redrawn before inductors are eliminated so that the cut-set encircles one node only, and this is sometimes inconvenient.

APPENDIX A

Example of Partitioning

For the example of Fig. 2(a), the transformed circuit without inductors is given in Fig. 2(b). (This is a theoretical problem and the circuit has no practical value.) This circuit is described by the equations

$$
\begin{array}{c}
\begin{array}{c} 1 \\ 2 \\ 3 \\ 4 \\ 5 \\ 6 \\ 7 \\ 8 \\ 9 \\ 10 \\ 11 \\ 12 \\ 13 \\ 14 \end{array}
\begin{bmatrix}
1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 & 10 & 11 & 12 & 13 & 14 \\
C_1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & C_2 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -C_2 & 0 & 0 & 0 & 0 \\
0 & 0 & L_1 & 0 & 0 & 0 & 0 & 0 & 0 & -L_1 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & C_6 & -C_6 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & -C_6 & C_6+C_7 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & L_2 & -L_2 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & -L_2 & L_2+C_3 & -C_3 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & -C_3 & C_3+C_4 & -C_4 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & -C_4 & C_4+C_5 & 0 & 0 & 0 & -C_5 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & C_2+L_1 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & C_7 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -C_8 & C_8+C_9 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0
\end{bmatrix}
\end{array}
\begin{bmatrix} v_1 \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ v_{14} \end{bmatrix}
=
$$

$$
\begin{array}{c}
\begin{matrix} 1 \\ 2 \\ 3 \\ 4 \\ 5 \\ 6 \\ 7 \\ 8 \\ 9 \\ 10 \\ 11 \\ 12 \\ 13 \\ 14 \end{matrix}
\begin{bmatrix}
I_1 \\
-k_2C_2(\dot{v}_{10}-\dot{v}_2) \\
0 \\
0 \\
0 \\
0 \\
0 \\
k_3i_{10} \\
-I_1 \\
k_2C_2(\dot{v}_{10}-\dot{v}_2) \\
0 \\
0 \\
I_2-k_3v_{10}
\end{bmatrix}
\end{array}
=
\begin{array}{c}
\begin{matrix} 1 & & 2 & & 3 & & 4 & & 5 & & 6 & & 7 & & 8 & & 9 & & 10 & & 11 & & 12 & & 13 & & 14 \end{matrix}
\begin{bmatrix}
G_2 & & 0 & & 0 & & -G_2 & & 0 & & 0 & & 0 & & 0 & & 0 & & 0 & & 0 & & 0 & & 0 & & 0 \\
0 & & G_3+G_6 & & 1 & & -G_3 & & 0 & & 0 & & 0 & & 0 & & 0 & & -1 & & -G_6 & & 0 & & 0 & & 0 \\
0 & & -1 & & 0 & & G_2+G_3 & & 0 & & 0 & & 0 & & 0 & & 0 & & 1 & & 0 & & 0 & & 0 & & 0 \\
-G_2 & & -G_3 & & 0 & & 0 & & G_4 & & 0 & & 0 & & 0 & & 0 & & 0 & & 0 & & 0 & & 0 & & 0 \\
0 & & 0 & & 0 & & 0 & & 0 & & -1 & & 0 & & 0 & & 0 & & 0 & & -G_6 & & 0 & & 0 & & 0 \\
0 & & 0 & & 0 & & 0 & & 0 & & 0 & & 1 & & 0 & & 0 & & 0 & & 0 & & 0 & & 0 & & 0 \\
0 & & 0 & & 0 & & 0 & & 0 & & 0 & & 0 & & G_{10} & & 0 & & 0 & & 0 & & 0 & & 0 & & 0 \\
0 & & 0 & & 0 & & 0 & & 0 & & 0 & & 0 & & 0 & & 0 & & G_8+G_9 & & 0 & & 0 & & 0 & & 0 \\
0 & & 1 & & -1 & & 0 & & -G_4 & & 0 & & 0 & & 0 & & 0 & & 0 & & G_4+G_5+G_6 & & 0 & & 0 & & 0 \\
0 & & -G_5 & & 0 & & 0 & & 0 & & 0 & & 0 & & 0 & & 0 & & 0 & & 0 & & G_1 & & -G_6 & & -G_7 \\
0 & & 0 & & 0 & & 0 & & 0 & & 0 & & 0 & & 0 & & 0 & & 0 & & -G_6 & & 0 & & G_6+G_7 & & G_7+G_9 \\
0 & & 0 & & 0 & & 0 & & 0 & & 1 & & -1 & & 0 & & 0 & & -G_9 & & 0 & & 0 & & -G_7 & & 0
\end{bmatrix}
\end{array}
\begin{bmatrix} v_1 \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ v_{14} \end{bmatrix}
$$

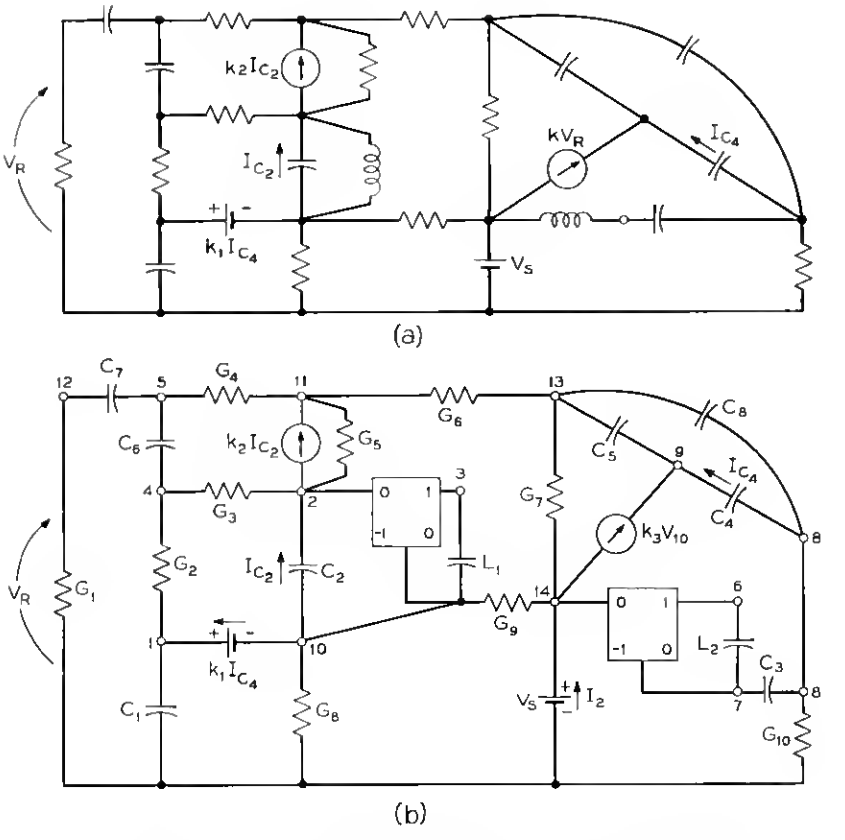

Fig. 2 — Circuit to demonstrate transformation and partitioning.

where I_1 and I_2 are the unbalance currents due to the vs's and

$$v_{14} = V_S .$$

Notice that except for degenerate cases (for example, if $C_6 = 0$), the order of complexity of this network is 9.

APPENDIX B

Matrix Reduction

Consider the partitioned form of equation (1). The section **n5** can be eliminated as follows: for an IVS of α volts connected between nodes k

and l (node k is in section **n5**, node l is not)

$$v_k = v_l + \alpha.$$

For a VDVS or CDVSR connected between nodes k and l, where the vs is dependent on the voltage vector $\mathbf{v}_m$ (each voltage of $\mathbf{v}_m$ is not in section **n5**).

$$v_k = v_l + \beta \mathbf{v}_m.$$

Thus the system can be reduced to

$$\begin{array}{c} \\ \mathbf{n1} \\ \mathbf{n2} \\ \mathbf{n3} \\ \mathbf{n4} \end{array} \begin{array}{c} \begin{array}{cccc} \mathbf{n1} & \mathbf{n2} & \mathbf{n3} & \mathbf{n4} \end{array} \\ \begin{bmatrix} C_{11} & C_{12} & C_{13} & 0 \\ C_{21} & C_{22} & C_{23} & 0 \\ C_{31} & C_{32} & C_{33} & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \end{array} \begin{bmatrix} \dot{\mathbf{v}}1 \\ \dot{\mathbf{v}}2 \\ \dot{\mathbf{v}}3 \\ \dot{\mathbf{v}}4 \end{bmatrix} = \begin{bmatrix} \mathbf{i}1 \\ \mathbf{i}2 \\ \mathbf{i}3 \\ \mathbf{i}4 \end{bmatrix} - \begin{bmatrix} G_{11} & G_{12} & G_{13} & G_{14} \\ G_{21} & G_{22} & G_{23} & G_{24} \\ G_{31} & G_{32} & G_{33} & G_{34} \\ G_{41} & G_{42} & G_{43} & G_{44} \end{bmatrix} \begin{bmatrix} \mathbf{v}1 \\ \mathbf{v}2 \\ \mathbf{v}3 \\ \mathbf{v}4 \end{bmatrix}. \quad (3)$$

Nodes **n4** can be eliminated by first writing part of equation (3) as

$$\mathbf{v}4 = G_{44}^{-1} \left\{ \mathbf{i}4 - [G_{41}\ G_{42}\ G_{43}] \begin{bmatrix} \mathbf{v}1 \\ \mathbf{v}2 \\ \mathbf{v}3 \end{bmatrix} \right\} \quad (4)$$

Thus

$$\begin{aligned} \begin{bmatrix} C_{11} & C_{12} & C_{13} \\ C_{21} & C_{22} & C_{23} \\ C_{31} & C_{32} & C_{33} \end{bmatrix} \begin{bmatrix} \dot{\mathbf{v}}1 \\ \dot{\mathbf{v}}2 \\ \dot{\mathbf{v}}3 \end{bmatrix} &= \begin{bmatrix} \mathbf{i}1 \\ \mathbf{i}2 \\ \mathbf{i}3 \end{bmatrix} - \begin{bmatrix} G_{11} & G_{12} & G_{13} \\ G_{21} & G_{22} & G_{23} \\ G_{31} & G_{32} & G_{33} \end{bmatrix} \begin{bmatrix} \mathbf{v}1 \\ \mathbf{v}2 \\ \mathbf{v}3 \end{bmatrix} - \begin{bmatrix} G_{14} \\ G_{24} \\ G_{34} \end{bmatrix} \mathbf{v}4 \\ &= \begin{bmatrix} \mathbf{it}1 \\ \mathbf{it}2 \\ \mathbf{it}3 \end{bmatrix} - \begin{bmatrix} G1_{11} & G1_{12} & G1_{13} \\ G1_{21} & G1_{22} & G1_{23} \\ G1_{31} & G1_{32} & G1_{33} \end{bmatrix} \begin{bmatrix} \mathbf{v}1 \\ \mathbf{v}2 \\ \mathbf{v}3 \end{bmatrix}. \end{aligned} \quad (5)$$

The matrix

$$\begin{bmatrix} C_{11} & C_{12} & C_{13} \\ C_{21} & C_{22} & C_{23} \\ C_{31} & C_{32} & C_{33} \end{bmatrix}$$

has order **n1** + **n2** + **n3** and rank no greater than **n1** + **n2**. The **n3**

linearly dependent rows and columns can be deleted from equation (5) by adding selected rows in the section **n1** and **n2** to rows in the range **n3**. The selection is made as follows: starting with any row in the section **n3**, examine the first entry. If it is nonzero add row 1 to this row. Continue along the row, repeating if necessary, until all the entries are zero. Proceed for the other dependent rows. Equation (5) can then be written as

$$\begin{bmatrix} C_{11} & C_{12} & C_{13} \\ & & \\ C_{21} & C_{22} & C_{23} \end{bmatrix} \begin{bmatrix} \dot{\mathbf{v}}1 \\ \dot{\mathbf{v}}2 \\ \dot{\mathbf{v}}3 \end{bmatrix} = \begin{bmatrix} \mathbf{it}1 \\ \\ \mathbf{it}2 \end{bmatrix} - \begin{bmatrix} G1_{11} & G1_{12} & G1_{13} \\ & & \\ G1_{21} & G1_{22} & G1_{23} \end{bmatrix} \begin{bmatrix} \mathbf{v}1 \\ \mathbf{v}2 \\ \mathbf{v}3 \end{bmatrix} \tag{6}$$

and

$$\mathbf{v}3 = G1_{33}'^{-1} \left\{ \mathbf{it}3' - [G1_{31}' \; G1_{32}'] \begin{bmatrix} \mathbf{v}1 \\ \mathbf{v}2 \end{bmatrix} \right\}. \tag{7}$$

It is a simple process for the reader to prove to himself that eliminating a node of a floating capacitor subgraph which is part of a GCSET as described above yields the same result as equating the algebraic sum of the voltages across the capacitors in the GCSET to zero (analogous to the algebraic sum of the currents entering the inductor cut-set node through the inductors adding up to zero).

Substituting equation (7) and its derivative into equation (6) we obtain

$$\begin{bmatrix} C2_{11} & C2_{12} \\ C2_{21} & C2_{22} \end{bmatrix} \begin{bmatrix} \dot{\mathbf{v}}1 \\ \dot{\mathbf{v}}2 \end{bmatrix} = \begin{bmatrix} \mathbf{ip}1 \\ \mathbf{ip}2 \end{bmatrix} - \begin{bmatrix} G2_{11} & G2_{12} \\ G2_{21} & G2_{22} \end{bmatrix} \begin{bmatrix} \mathbf{v}1 \\ \mathbf{v}2 \end{bmatrix}. \tag{8}$$

The total number of restrictions have not yet been placed on the network.

(*i*) For a DVS imbedded in a capacitor chain or a CDVSC free of capacitors on one node connected between nodes k and l, where node k is specified in section **n2**,

$$v_k = v_l + \gamma \mathbf{v}_i$$

or

$$v_k = v_l + v\dot{\mathbf{v}}_i$$

where $\mathbf{v}_i$ is the set of voltages upon which the source is dependent. A particular voltage of $\mathbf{v}_i$ may be in any section **n1**, **n2**, **n3**, **n4**, or **n5**.

(*ii*) For a CDCSC connected between nodes k and l, the currents I_k and I_l injected into nodes k and l with the CDCSC removed must be modified to

$$I_k + \eta\dot{\mathbf{v}}_j$$

and

$$I_l - \eta\dot{\mathbf{v}}_j,$$

respectively, where η has the dimensions of farads.

(*iii*) For a GCSET with node j of the capacitor tree containing the GCSET specified in section **n2**, node j is eliminated as follows: examine the entries of row j of the remaining capacitance matrix. If entry $C_{j,l} \neq 0$, subtract $C_{j,l}/C_{l,l}$ times row l from row j, where $l = 1, p$; p is the order of **n1** + **n2**. Thus row j is reduced to a row of zeros.

The system can now be written as

$$[C]\dot{\mathbf{v}}\mathbf{1} = \mathbf{iF1} - [G]\mathbf{v1}. \tag{9}$$

Barring degeneracy, matrix C is nonsingular with rank **n1**.

APPENDIX C

Example of the Method

For the circuit of Fig. 3 (the example of C. Pottle[9]), nodes 1, 2, and 3 are placed in the **n1** section, and node 4 is placed in the **n5** section. Thus, by inspection

$$\begin{bmatrix} C_1 + C_4 & 0 & 0 & -C_4 \\ 0 & C_2 & 0 & 0 \\ 0 & 0 & C_3 & 0 \\ -C_4 & 0 & 0 & C_4 \end{bmatrix} \begin{bmatrix} \dot{v}_1 \\ \dot{v}_2 \\ \dot{v}_3 \\ \dot{v}_4 \end{bmatrix} = \begin{bmatrix} -2C_4(\dot{v}_4 - \dot{v}_1) - 2G_2(v_2 - v_1) \\ 0 \\ 0 \\ I_1 \end{bmatrix}$$

$$- \begin{bmatrix} G_2 + G_3 & -G_2 & -G_3 & 0 \\ -G_2 & G_1 + G_2 & 0 & -G_1 \\ -G_3 & 0 & G_3 - G_4 & 0 \\ 0 & -G_1 & 0 & G_1 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix}$$

where

$$v_4 = E;\ \dot{v}_4 = \dot{E}.$$

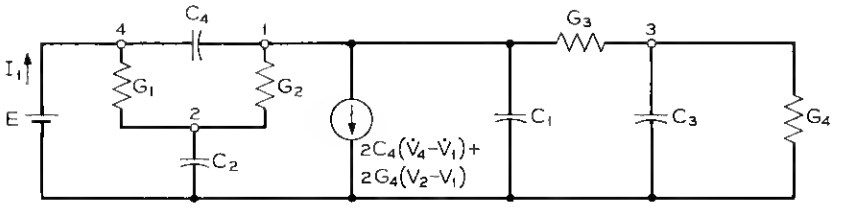

Fig. 3 — Example of Appendix C.

The derivative of the source E must be considered if a capacitor is connected to both of its nodes. Clearing out the voltage terms in the current array,

$$\begin{bmatrix} C_1 - C_4 & 0 & 0 & C_4 \\ 0 & C_2 & 0 & 0 \\ 0 & 0 & C_3 & 0 \\ -C_4 & 0 & 0 & C_4 \end{bmatrix} \begin{bmatrix} \dot{v}_1 \\ \dot{v}_2 \\ \dot{v}_3 \\ \dot{v}_4 \end{bmatrix}$$

$$= \begin{bmatrix} 0 \\ 0 \\ 0 \\ I_1 \end{bmatrix} - \begin{bmatrix} G_3 - G_2 & G_2 & -G_3 & 0 \\ -G_2 & G_1 + G_2 & 0 & -G_1 \\ -G_3 & 0 & G_3 + G_2 & 0 \\ 0 & -G_1 & 0 & G_1 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix}.$$

Eliminating v_4 and $\dot{v}_4$ as described in Appendix B,

$$\begin{bmatrix} C_1 - C_4 & 2C_4 & 0 \\ 0 & C_2 & 0 \\ 0 & 0 & C_3 \end{bmatrix} \begin{bmatrix} \dot{v}_1 \\ \dot{v}_2 \\ \dot{v}_3 \end{bmatrix} = \begin{bmatrix} -C_4\dot{E} \\ G_1E \\ 0 \end{bmatrix} - \begin{bmatrix} G_3 - G_2 & G_2 & -G_3 \\ -G_2 & G_1 + G_2 & 0 \\ -G_3 & 0 & G_3 + G_4 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix}.$$

This is as far as we can go symbolically and as far as the method takes us. Normally all that remains is a simple inversion of the remaining capacitance matrix, but Pottle chose $C_1 = C_4$. This makes the capacitance matrix singular and so another node must be eliminated. Eliminating node 1,

$$\begin{bmatrix} C_2 + \dfrac{2C_4C_2}{G_3 - G_2} & 0 \\ \dfrac{2C_4G_3}{-G_2} & C_3 \end{bmatrix} \begin{bmatrix} \dot{v}_2 \\ \dot{v}_3 \end{bmatrix} = \begin{bmatrix} G_1E + \dfrac{C_4G_2}{G_3 - G_2}\dot{E} \\ \dfrac{C_4G_3}{G_3 - G_2}\dot{E} \end{bmatrix}$$

$$-\begin{bmatrix} G_1 + G_2 + \dfrac{G_2^2}{G_3 - G_2} & -\dfrac{G_2 G_3}{G_3 - G_2} \\ \dfrac{G_2 G_3}{G_3 - G_2} & G_3 + G_4 - \dfrac{G_3^2}{G_3 - G_2} \end{bmatrix} \begin{bmatrix} v_2 \\ v_3 \end{bmatrix}.$$

The vector

$$\begin{bmatrix} \dot{v}_2 \\ \dot{v}_3 \end{bmatrix}$$

can now be expressed explicitly.

REFERENCES

1. Bashkow, T. R., "The A Matrix, New Network Description," IRE Trans. Circuit Theory, *CT-4*, No. 3 (September 1967), pp. 117–119.
2. Bryant, P. R., "The Explicit Form of Bashkow's A Matrix," IRE Trans. Circuit Theory, *CT-9*, No. 3 (September 1962), pp. 303–306.
3. Kuh, E. S., "Stability of Linear Time-Varying Networks—The State Space Approach," IEEE Trans. Circuit Theory, *CT-12*, No. 2 (June 1965), pp. 150–157.
4. Roe, P. H., "Formulation of the State Equations for Electric and Electronic Circuit," Proc. 1963 Sixth Midwest Symp. on Circuit Theory, pp. R1–R16, University of Wisconsin, Madison, Wisc.
5. Kuh, E. S. and Rohrer, R. A., "The State-Variable Approach to Network Analysis," Proc. IEEE, *53*, No. 7 (July 1965), pp. 672–686.
6. Purslow, E. J. and Spence, R., "Order of Complexity of Active Networks," Proc. IEE, February 1967, *114*, No. 2, pp. 195–198.
7. Tow, J., "On the Order of Complexity of Linear Active Networks," Proc. IEE (London) September 1968.
8. Miller, J. A. and Newcomb, R. W., "Determination of the State-Variable Equations for Admittance Descriptions Suitable for the Computer," Proc. IEEE, *56*, No. 8 (August 1968), pp. 1372–1373.
9. Pottle, C., "State-Space Techniques for General Active Network Analysis," Chapter 7 of *System Analysis by Digital Computer*, ed. F. F. Kuo and J. F. Kaiser, New York: John Wiley and Sons, 1966.